Service aware Access Networks through Network Processor Technology

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Outline

> Introduction
  - Service aware Access Networks
  - Service enablers
  - Requirements

> Network Processor Technology

> Service aware Access Networks through NPU Technology

> Conclusions and future work
Introduction: Service aware Access Networks

Requirements:

> Multiple subscriber devices / CPN
> CPN Autoconfiguration
> High bandwidth
> Nomadism
> Secure

> New services (triple play)
  - Packet oriented
  - IP awareness closer to end user
Introduction: Firewall / NAPT service

Service Enabler: Packet Classification

Connection tracking module
Increase functional intelligence of the Access Network

> L3(+) awareness closer to the CPN
> Identify & implement interesting services
> Identify & implement enablers for these and future services

→ *Access devices require more computational power!!*
Outline

- Introduction
- Network Processor Technology
  - Definition
  - Intel 2nd generation NPU: IXP2400
  - Programming model
- Service aware Access Networks through NPU Technology
- Conclusions and future work
## Network Processor Technology

Increasing need for powerful and flexible network systems:

<table>
<thead>
<tr>
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<th>GPP – based solutions</th>
<th>ASIC – based solutions</th>
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<tbody>
<tr>
<td></td>
<td>(General Purpose Processor)</td>
<td>(Custom silicon)</td>
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<tr>
<td><strong>Pro</strong></td>
<td>&gt; <strong>Programmability: flexible</strong></td>
<td>&gt; <strong>Fast</strong></td>
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<tr>
<td></td>
<td>&gt; Component reuse</td>
<td>&gt; <strong>Low power consumption</strong></td>
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<tr>
<td></td>
<td>&gt; <strong>Relatively low cost (RISC)</strong></td>
<td>&gt; <strong>Highly scalable</strong></td>
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<tr>
<td><strong>Con</strong></td>
<td>&gt; <strong>Rather slow</strong></td>
<td>&gt; <strong>Long time to market</strong></td>
</tr>
<tr>
<td></td>
<td>&gt; <strong>High power consumption</strong></td>
<td>&gt; <strong>High cost</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td>&gt; <strong>Inflexible: little reuse</strong></td>
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Network Processor Technology

Next generation network systems:

> Require a technology that has the advantages of custom silicon without the disadvantages:
  • High speed @ low power consumption
  • High scalability and reusability
  • Flexibility through programmability
  • Low cost

> The solution: Network Processors (NPU)
  • e.g. Intel’s 2\textsuperscript{nd} generation Network Processors: IXP2xx0
Radisys ENP-2611: IXP2400 evaluation board
Radisys ENP-2611: IXP2400 evaluation board
Receive / process / transmit paradigm
• Different tasks on different processing units with queues in between

> Microengines can run
• a series of sequential processing tasks (pipelined);
• a pool of parallel processing tasks;
• a mixture of both.
IXP2400: IXA Portability Framework

XScale core (OS=linux)

Packet processing ACE config

Packet processing ACE IDL interface

Object Management System (OMS)

Ingress interface ACE

Packet processing ACE

Packet processing ACE

Egress interface ACE

Resource Manager (RM)

Micro-Engine #1

Microblock group

Ingress interface microblock

Packet processing microblock

Micro-Engine #2

Packet processing microblock

Micro-Engine #n

Egress interface microblock

Input port

Output port

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Outline

> Introduction

> Network Processor Technology

> Service aware Access Networks through NPU Technology
  • Implementation details: firewall / NAPT on IXP2400
  • Performance analysis

> Conclusions and future work
Mapping Firewall / NAPT on IXP2400 hardware

Threads:

> Memory allocation
> Free memory
> Search for conntracks that timed out
> Allocation of TCP ports for NAPT
> Allocation of UDP ports for NAPT
> Allocation of ICMP ID’s for NAPT.

Multiple copies of packet classification code to increase performance
Performance Analysis

> Using Spirent Smartbits 6000

> GbE speed, minimum sized packets → 1,488,095 packets / s
  • Packet inter arrival time: 672 ns → 403 cycles / packet (600 MHz)

> All packets belong to a single connection

> All packets are classified
  • Firewall MEs process all packets
  • Packet matches last rule (all rules are processed!)
Performance Analysis Results: multithreading

Rules in local memory

Rules in SRAM
Performance Analysis Results

Headroom → Optimize Packet Classification Algorithm

Graph showing the relationship between the number of rules and throughput for different memory configurations. The graph indicates that as the number of rules increases, the throughput decreases, highlighting the need for optimization.
Conclusions and future work

> Evaluation of suitability and performance of network processors for increasing application awareness and intelligence in IP network nodes

> Test case:
  • Netfilter based firewall / NAPT implementation on Intel IXP2400
  • SRAM memory can sustain up to 12 threads in parallel
  • Up to 23 rules / packet @ GbE speed
  • Processing power headroom (cf. static implementation)

> Future work:
  • Other packet classification algorithms might increase performance