An Asymmetric Passive Optical Network: A Combined Point-to-Point and Passive-Optical-Network

Report from MUSE subproject D

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Outline

- Rationale
- MUSE Reference Architecture
- Architecture of the Asymmetrical PON
- Prototype of the Platform
- FPGA Implementation
- Scheduler
- Summary
Architecture of the Asymmetrical PON

PON:
- Needs MAC and complex OAM
- High line rate and low user bandwidth
- Low on installed fiber
- Native multicasting

Point to Point
- Power consumption
- Fiber and components
- Line rate matches user bandwidth
- Secure

AsPON
- Native multicasting
- Use of commercially available NICs
- Low power consumption
- Placed in CO and in the field
- Medium fiber usage

![Architecture of the Asymmetrical PON diagram]
## Electro-optics: Downlink Transceivers

<table>
<thead>
<tr>
<th>48 downlinks @ 100 Mb/s Optics</th>
<th>P2P</th>
<th>AsPON</th>
<th>Saving</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dissipation</td>
<td>48 SFF FE</td>
<td>5 SFP GbE + 4 PORx</td>
<td>86%</td>
</tr>
<tr>
<td>Footprint (width)</td>
<td>67 cm</td>
<td>15 cm</td>
<td>77%</td>
</tr>
<tr>
<td></td>
<td>48 W</td>
<td>7 W</td>
<td></td>
</tr>
</tbody>
</table>

12 ports
Prototype Block Diagram

Features:
- Six individual or cascaded sections
- 1Gbit/s per eight users
- Aggregation up to 6 Gbit/s
- Use of normal ethernet MAC protocols
- No additional data bus for payload between FPGAs
- Ethernet data plane
- Distributed management system
- Multiple transmitters for downstream PONs
- More flexible power budget

MAC
FPGA
SFP
memory, timing, power, etc.

8x RX
switch

1 2 3 6

to metro

from 8x CPE

1 8 9 10 16 17 24

from 8x CPE

1 2 3 8 9 16 17 24

from 8x CPE

40 48

from 8x CPE

1 2 3 n

to 48x CPE

to LSC
Prototype of the Platform

- Power Supply
- QDR Memory
- Virtex 4 LX100
- Configuration
- Clock

10 port MAC  GbE SFP  12 RX array

- 14 layer PCB
- 4 power rails
- 48 ports in 6 clusters of 8 users
- < 5W per user (worse case)
- Producible PCB (feature & insulation)
FPGA Implementation (1/2)
FPGA Implementation (2/2)

- Resource Control Enforcement Function
  - Content Addressable Memory checks frames against:
    - MAC port
    - Customer VLAN id,
    - Protocol,
    - IP source address, IP destination address,
    - IP source port, and IP destination port
  - On a match it will do either:
    - Pass without modification
    - Replace C-VLAN tag by S-VLAN tag. If packet has no C-VLAN tag then it will be dropped.
    - Insert S-VLAN tag, double tagging
    - Drop packet (default when there is no match)

- Classifier
  - Mapping of packet to flows for end-to-end QoS
  - Three p-bits of S-VLAN for four QoS classes
- Peak-rate and burst-size based policing
LC2WFQ Scheduler

- Huge Differentiation in Services and QoS Requirements
- Decentralized Control
- Design Considerations:
  - Fairness
  - Low Latency (bounded)
  - Time Complexity
  - Design Complexity
  - Distributed Design
- Round Robin versus Weighted Fair Queuing
LC2WFQ Scheduler (simulation)

(Port 1,12,23: 64B. Port 2,13,24: 512B. Rest: 64-1500B. All ports: 41.6Mb/s)
LC2WFQ Scheduler (simulation)
(Port 10 and 21 Misbehave (200Mb/s instead of 41.6 Mb/s)
Distributed Scheduler

FPGA\textsubscript{n}

Queue Management

Scheduler Control

Flow Selection

Flow Selection Logic

to/from FPGA\textsubscript{n-1}

packet size
front end
packet size
Flow\_Control\textsubscript{0}
range
active
credit

shift register

shift\_in
reset\_out

reset\_out
stop\_out
read\_strobe
read\_done
start\_out
stop\_in

packet size
front end
packet size
Flow\_Control\textsubscript{M}
range
active
credit

shift register

adress encoder

shift\_out
reset\_in

to/from FPGA\textsubscript{n+1}
Summary

- AsPON Combines the best features of *Point-to-Point* and *PON* technology
- Created a prototype using commercially available components
- Single Ethernet plane for interconnecting FPGAs
- Designed and implemented a novel scheduler
- Successfully tested AsPON concentrator
- Foundation for advanced L2+ functions (Dec ’07)
Thank You!

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http://www.ist-muse.eu